Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		("(microadjstructuremicrostructure)with(gripermanipulator)").PN	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/30 13:36
L1	62	triple adj gate with (mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:32
L2	393884	"2" and (triple adj gate mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 13:12
L3	62	1 and (triple adj gate mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:32
L4	1	triple adj gate with (mosfet transistor).ti.	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:34
L5	14	((triple tri multi) adj gate) with (mosfet transistor).ti.	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:44
L6	128	((i h) adj shape$2) with (mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:37
L7	277	((triple tri multi) adj gate) with (mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:50
L8	514	((triple tri i h) adj gate) with (mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:50
L9	4954	((triple tri i h) near4 gate) with (mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:50
L10	369	((triple tri) near4 gate) with (mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 14:52
L11	98	((triple tri) near gate) with (mosfet transistor)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 15:28
L12	19	((triple tri) near gate).ti.	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/08 15:28

S1	71993	(method process$3) with (side adj wall sidewall spacer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/06/06 10:43
S2	10472	((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:43
S3	8483	(((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and ((etch$3) with (side adj wall sidewall spacer))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:44
S4	3612	(((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:42
S5	1636	((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S6	1636	(((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45

S7	364	((((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)) and ((rotation$2 rotat$2 rotating spin$4 turning turn$3) with substrate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:50
S8	99	(((((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)) and ((rotation$2 rotat$2 rotating spin$4 turning turn$3) with substrate)) and (acid with etch$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:51
S9	10135	(method process$3) with ((side adj wall sidewall spacer) with (gate transistor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:41
S10	28954	((side adj wall sidewall spacer) with (gate transistor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:43
S11	22184	(((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:44

S12	13851	((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S13	4977	(((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:46
S14	4977	((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch$2 gate insulat$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:48
S15	2079	(((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch$2 gate insulat$3)) and (wet near5 etch$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:48

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L11: (98) ((triple tri) near gate) with (mosfet transistor)

L12: (19) ((triple tri) near gate).ti

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DBs US-PGPUB; USPAT; EPO; JPO Buses

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P	2	3	4	5
6	☑	☐	US 20040036127	20040226	27	Tri-gate devices and methods of fabrication	257/401	257/E21.415; 257/E29.137;		Chau, Robert S. et al.	☐	☐	☐	☐	☐	☐	☐
7	☑	☐	US 20040036126	20040226	20	Tri-gate devices and methods of fabrication	257/401	257/E21.415; 257/E29.137;		Chau, Robert S. et al.	☐	☐	☐	☐	☐	☐	☐
8	☑	☐	US 20030136963	20030724	15	Self-aligned triple gate silicon-on-insulator (SOI) de	257/59	257/E21.415; 257/E21.442;		Krivokapic, Zoran et al.	☐	☐	☐	☐	☐	☐	☐
9	☑	☐	US 6727546 B2	20040427	15	Self-aligned triple gate silicon-on-insulator (SOI) de	257/331	257/347; 257/365;		Krivokapic; Zoran et al.	☐	☐	☐	☐	☐	☐	☐
10	☑	☐	US 6716684 B1	20040406	16	Method of making a self-aligned triple gate silicon-	438/157	257/E21.415; 257/E21.442;		Krivokapic; Zoran et al.	☐	☐	☐	☐	☐	☐	☐
11	☑	☐	US 6670248 B1	20031230		Triple gate oxide process with high-k gate dielectric	438/287	257/E21.193; 257/E29.162;		Ang; Chew Hoe et al.	☐	☐	☐	☐	☐	☐	☐
12	☑	☐	US 6268251 B1	20010731		Method of forming MOS/CMOS devices with dua	438/275	257/E21.625; 438/981		Zhong; Dong et al.	☐	☐	☐	☐	☐	☐	☐
13	☑	☐	US 6184546 B1	20010206	7	High barrier gate and tri-step doped channel field-effect tra	257/192	257/12; 257/194;		Liu; W. C. et al.	☐	☐	☐	☐	☐	☐	☐
14	☑	☐	US 5679970 A	19971021		Triple gate flash-type EEPROM memory and its pro	257/320	257/E21.682; 257/E27.103		Hartmann; Joel	☐	☐	☐	☐	☐	☐	☐
15	☑	☐	US 4561467 A	19851231		Triple gate valve assembly	137/624.18	137/614.14; 137/624.13;		Rouse; Michael W. et al.	☐	☐	☐	☐	☐	☐	☐
16	☑	☐	US 2485886 A	19491025		Triple gate [TEXT AVAILABLE IN USOCR DA	327/414	341/173; 370/534		JOHNSTONE CHARLES W et al.	☐	☐	☐	☐	☐	☐	☐
17	☑	☐	JP 2004134754 A	20040430		PROCESS FOR FORMING TRIPLE GATE OXIDE FILM				ANG, CHEW HOE et al.	☐	☐	☐	☐	☐	☐	☐
18	☑	☐	WO 9401892 A1	19940120		TRIPLE-GATE FLASH EEPROM MEMORY AND M		257/315; 257/E21.682;		HARTMANN, JOEL	☐	☐	☐	☐	☐	☐	☐
19	☑	☐	DE 3778474 A1	19920527		Triple gate optical star coupler					☐	☐	☐	☐	☐	☐	☐

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